Intel® Next Generation Microarchitecture Codename Haswell: New Processor Innovations

Bob Valentine, Sr. Principal Engineer, Intel
Agenda

• Introduction
• Intel® Microarchitecture (Haswell): Core
• Haswell: Cache Hierarchy and Interconnects
• Haswell: Power Management
• Wrap Up
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• Intel® Microarchitecture (Haswell): Core
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Haswell builds upon innovations in the 2nd and 3rd Generation Intel® Core™ i3/i5/i7 Processors (Sandy Bridge and Ivy Bridge)
Haswell “Philosophy”

Converged core, Scalable Platform

1. Converged core, Scalable Platform

2. More performance per core
   - Single Thread Instructions Per Cycle (broad workload mixture)
   - 2004 to 2013

3. Flat or decreasing power envelopes
   - Power Envelopes for Comparable Segments
   - Mainstream
   - Lowest

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Intel® Microarchitecture (Haswell)
Sandy Bridge (Tock): Recap

Next Generation Intel® Turbo Boost Technology

High Bandwidth Last Level Cache

Processor Graphics and Media

Embedded DisplayPort* (DP)

Discrete Graphics Support: 1x16 or 2x8

Energy Efficiency

Stunning Performance

CPU, Graphics, MC, PCI Express* On Single Chip

High BW/low-latency modular core/Graphic interconnect

Substantial performance improvement

Intel® Advanced Vector Extension (Intel® AVX)

Integrated Memory Controller 2ch DDR3

Intel® Hyper-Threading Technology
4 Cores / 8 Threads
2 Cores / 4 Threads
Ivy Bridge (Tick): Recap

- Built on Sandy Bridge Microarchitecture
- 22nm Process Technology
- Next Generation Processor Graphics and Media (Microsoft* DirectX*11)
- Intel® Secure Key (Digital Random Number Generator)
- Solid performance improvement per core
- Intel® Advanced Vector Extensions (Intel® AVX) 16-bit floating point format
- Intel® OS Guard (Supervisor Mode Execution Protection)
- Socket compatibility with Sandy Bridge

3rd Generation Intel® Core™ Microarchitecture (Ivy Bridge)
On to Haswell microarchitecture...
Agenda

• Introduction

• **Intel® Microarchitecture (Haswell): Core**
  – Compute innovation and Intel® AVX2
  – Enhanced security primitives
  – Synchronization improvements and Intel® TSX
  – Virtualization performance and EPT

• Haswell: Cache Hierarchy and Interconnects

• Haswell: Power Management

• Wrap Up
Haswell Core at a Glance

Next generation branch prediction
• Improves performance and saves wasted work

Improved front-end
• Initiate TLB and cache misses speculatively
• Handle cache misses in parallel to hide latency
• Leverages improved branch prediction

Deeper buffers
• Extract more instruction parallelism
• More resources when running a single thread

More execution units, shorter latencies
• Power down when not in use

More load/store bandwidth
• Better prefetching, better cache line split latency & throughput, double L2 bandwidth
• New modes save power without losing performance

No pipeline growth
• Same branch misprediction latency
• Same L1/L2 cache latency
### Haswell Buffer Sizes

Extract more parallelism in every generation

<table>
<thead>
<tr>
<th></th>
<th>Nehalem</th>
<th>Sandy Bridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Out-of-order Window</td>
<td>128</td>
<td>168</td>
<td>192</td>
</tr>
<tr>
<td>In-flight Loads</td>
<td>48</td>
<td>64</td>
<td>72</td>
</tr>
<tr>
<td>In-flight Stores</td>
<td>32</td>
<td>36</td>
<td>42</td>
</tr>
<tr>
<td>Scheduler Entries</td>
<td>36</td>
<td>54</td>
<td>60</td>
</tr>
<tr>
<td>Integer Register File</td>
<td>N/A</td>
<td>160</td>
<td>168</td>
</tr>
<tr>
<td>FP Register File</td>
<td>N/A</td>
<td>144</td>
<td>168</td>
</tr>
<tr>
<td>Allocation Queue</td>
<td>28/thread</td>
<td>28/thread</td>
<td>56</td>
</tr>
</tbody>
</table>
Haswell Execution Unit Overview

Unified Reservation Station

Port 0
- Integer ALU & Shift
- FMA FP Multiply
- Vector Int Multiply
- Vector Logicals
- Branch
- Divide
- Vector Shifts

Port 1
- Integer ALU & LEA
- FMA FP Multi
- FP Add
- Vector Int ALU
- Vector Logicals

Port 2
- Load & Store Address

Port 3
- Store Data

Port 4
- Integer ALU & LEA

Port 5
- Integer ALU & Shift

Port 6
- Vector Shuffle

Port 7
- Store Address

2xFMA
- Doubles peak FLOPs
- Two FP multiplies benefits legacy

4th ALU
- Great for integer workloads
- Frees Port0 & 1 for vector

New Branch Unit
- Reduces Port0 Conflicts
- 2nd EU for high branch code

New AGU for Stores
- Leaves Port 2 & 3 open for Loads

Intel® Microarchitecture (Haswell)
Haswell New Compute Instructions

• Intel® Advanced Vector Extensions 2 (Intel® AVX2)
  - Includes
    ▪ 256-bit Integer vectors
    ▪ FMA: Fused Multiply-Add
    ▪ Full-width element permutes
    ▪ Gather
  - Benefits
    ▪ High performance computing
    ▪ Audio & Video
    ▪ Games

• New Integer Instructions
  - Indexing and hashing
  - Cryptography
  - Endian conversion – MOVBE

• Full Instruction Specification Available at: http://software.intel.com/en-us/avx

<table>
<thead>
<tr>
<th>Group</th>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Field Pack/Extract</td>
<td>BZHI, SHLX, SHRX, SARX, BEXTR</td>
</tr>
<tr>
<td>Variable Bit Length Stream Decode</td>
<td>LZCNT, TZCNT, BLSR, BLSMSK, BLSI, ANDN</td>
</tr>
<tr>
<td>Bit Gather/Scatter</td>
<td>PDEP, PEXT</td>
</tr>
<tr>
<td>Arbitrary Precision Arithmetic &amp; Hashing</td>
<td>MULX, RORX</td>
</tr>
</tbody>
</table>
• 2 new FMA units provide 2x peak FLOPs/cycle of previous generation

• 2X cache bandwidth to feed wide vector units
  – 32-byte load/store for L1
  – 2x L2 bandwidth

• 5-cycle FMA latency same as an FP multiply

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.
## Core Cache Size/Latency/Bandwidth

<table>
<thead>
<tr>
<th>Metric</th>
<th>Nehalem</th>
<th>Sandy Bridge</th>
<th>Haswell</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Instruction Cache</td>
<td>32K, 4-way</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
</tr>
<tr>
<td>L1 Data Cache</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
<td>32K, 8-way</td>
</tr>
<tr>
<td>Fastest Load-to-use</td>
<td>4 cycles</td>
<td>4 cycles</td>
<td>4 cycles</td>
</tr>
<tr>
<td>Load bandwidth</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle (banked)</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>Store bandwidth</td>
<td>16 Bytes/cycle</td>
<td>16 Bytes/cycle</td>
<td>32 Bytes/cycle</td>
</tr>
<tr>
<td>L2 Unified Cache</td>
<td>256K, 8-way</td>
<td>256K, 8-way</td>
<td>256K, 8-way</td>
</tr>
<tr>
<td>Fastest load-to-use</td>
<td>10 cycles</td>
<td>11 cycles</td>
<td>11 cycles</td>
</tr>
<tr>
<td>Bandwidth to L1</td>
<td>32 Bytes/cycle</td>
<td>32 Bytes/cycle</td>
<td>64 Bytes/cycle</td>
</tr>
<tr>
<td>L1 Instruction TLB</td>
<td>4K: 128, 4-way 2M/4M: 7/</td>
<td>4K: 128, 4-way 2M/4M: 8/</td>
<td>4K: 128, 4-way 2M/4M: 8/</td>
</tr>
<tr>
<td></td>
<td>thread</td>
<td>thread</td>
<td></td>
</tr>
<tr>
<td>L1 Data TLB</td>
<td>4K: 64, 4-way 2M/4M: 32,</td>
<td>4K: 64, 4-way 2M/4M: 32,</td>
<td>4K: 64, 4-way 2M/4M: 32,</td>
</tr>
<tr>
<td></td>
<td>4-way 1G: fractured</td>
<td>4-way 1G: 4, 4-way</td>
<td>4-way 1G: 4, 4-way</td>
</tr>
<tr>
<td>L2 Unified TLB</td>
<td>4K: 512, 4-way</td>
<td>4K: 512, 4-way</td>
<td>4K+2M shared: 1024, 8-way</td>
</tr>
</tbody>
</table>

All caches use 64-byte lines
Enhanced Security Primitives

Cryptography protects nearly all data and transactions you want to keep secure.

Haswell’s microarchitecture improvements and new instructions enable substantial gains in cryptography.
Synchronization Improvements

- **Improving existing primitives**
  - Faster LOCK-prefixed instructions
  - A focus in recent generations

- **Locks still limit concurrency**
  - Lock-protected critical sections
  - Needed for threading correctness
  - Tradeoff: correctness vs. performance

- **Intel® TSX**
  - Target lock granularity optimizations
  - Lock Elision
    - Execute without acquiring locks
    - Performance of fine-grained locks with effort of coarse-grained locks

Intel® TSX exposes parallelism through Lock Elision
A Canonical Intel® TSX Execution

Thread 1

Acquire
Critical section
Release

Thread 2

Acquire
Critical section
Release

Hash Table

Lock remains free throughout

No serialization and no communication if no conflicts
Transactional Synchronization

• **Intel® TSX: Instruction set extensions for IA**
  - Transactionally execute lock-protected critical sections
  - Execute without acquiring lock → expose hidden concurrency
  - Hardware manages transactional updates – All or None
    ▪ Other threads can’t observe intermediate transactional updates
    ▪ If lock elision cannot succeed, restart execution & acquire lock

• **Efficient implementation eases developer enabling**
  - Simple and clean ISA interface for software developers to use
  - Competitive to typical uncontended critical sections
  - Designed to support typical critical sections transactionally
  - Hardware efficiently manages register and memory state

**Developer-friendly implementation**
Intel® TSX Interfaces for Lock Elision

• **Hardware Lock Elision (HLE) – XACQUIRE/XRELEASE**
  – Software uses legacy compatible hints to identify critical section. Hints ignored on hardware without TSX
  – Hardware support to execute transactionally without acquiring lock
  – Abort causes a re-execution without elision
  – Hardware manages all architectural state

• **Restricted Transactional Memory (RTM) – XBEGIN/XEND**
  – Software uses new instructions to specify critical sections
  – Similar to HLE but flexible interface for software to do lock elision
  – Abort transfers control to target specified by XBEGIN operand
  – Abort information returned in a general purpose register (EAX)

• **XTEST and XABORT – Additional instructions**
Virtualization on Haswell with Intel® VT

- Substantially improved guest/host transition times
- New *Accessed* and *Dirty* bits for Extended Page Tables (EPT) eliminates major cause of vmexits
- Overhauled TLB invalidations – lower latency, less serialization
- New VMFUNC instruction enables hyper-calls without a vmexit
- Intel® VT-d adds 4-level page walks to match Intel® VT-x

![Graph: Intel VT-x Roundtrip over Generations]

Haswell reduces round-trip to <500 cycles
Haswell Performance Monitoring Highlights

Precise Event-Based Sampling (PEBS) Enhancements

• New EventingIP entry for data profiling
• Data Linear Address provided for all PEBS memory events
  – Statistical memory address profiling outside of a debug environment

New Features Addressing Developer Requests

• Call Stack Mode for Last Branch Record (LBR)
  – Removes Call/Ret pairs to isolate call path that causes critical contentions
• Res_Programmed MSR
  – One-stop ‘In Use’ Status of Perfmon Fixed and GP Counters, PMI
  – Support for SW Virtualization/Sharing Protocol for Perfmon Resources
• Event updates, including:
  – Prefetch / Demand event clean-up
  – New Page Walker Load event for IA/EPT, instruction/data, data source
  – Page size info added to TLB events
• Intel® Transactional Synchronization Extension (Intel® TSX) support
  – Counters, LBRs, PEBS
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  – Background
  – Haswell Innovations
• Haswell: Power Management
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Cache, Interconnect, and System Agent: Background

- Haswell builds upon Sandy Bridge’s scalable interconnect and shared cache
  - Uni-directional ring with two stops for each core
  - Shared Last-Level Cache (LLC) scales with the number of cores
  - Processor graphics and system agent have separate ring stops
Cache, Interconnect, and System Agent: Haswell Innovations

- More access bandwidth per slice of shared LLC
  - New dedicated pipelines handle data and non-data accesses independently
- Improved load balancing to System Agent
  - Better credit-based management more efficiently shares resources
- Improved DRAM write throughput
  - Deeper pending queues: more decoupling, better scheduling
- Lower power, better efficiency
  - Focused effort to reduce idle and active power (next section)
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• Haswell: Power Management
  – Maximizing power-limited performance
  – Maximizing battery life
• Wrap Up
Maximizing Power-Limited Performance

• Extended operating range
  – Power efficient features: better than voltage / frequency scaling
  – Continued focus on gating unused logic and low-power modes
  – Optimized manufacturing and circuits

• Independent frequency domains
  – Cores separated from LLC+Ring for fine-grained control
  – Power Control Unit dynamically allocates budget when power-limited
  – Prioritization based on run-time characteristics selects domain with the highest performance return
Maximizing Battery Life

• Deeper idle states, lower active power
  – Continued focus on turning off blocks that are not required. Example: C7
    ▪ All clocks stopped, voltage removed from the majority of the CPU
    ▪ C7 engaged even when display is active
  – Faster state transition times by ~25%

• Smarter low power states
  – New S0ix idle states with idle power approaching tablet CPUs
  – More C-state intelligence
    ▪ System software request
    ▪ Time to next timer event
    ▪ Latency requirements
    ▪ Past history
    ▪ Run time hints from devices

Microarchitecture, power management, and manufacturing combine for 20x reduction in idle power!
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Summary

• Haswell is the next Intel® “tock” microarchitecture, builds upon Sandy Bridge to deliver:
  – **Scalability** across broad range of domains and workloads
  – **Per core performance** for the vast majority of workloads
  – **Lower power** for better performance and smaller envelopes

• Developer-friendly features
  – Fundamental performance and power improvements for legacy workloads, including AVX
  – New instructions addressing key developer requests
    ▪ Intel® AVX2 with FMA and 256-bit integer vectors
    ▪ Intel® Bit Manipulation Instructions
    ▪ Intel® TSX for thread parallelism through lock elision

• Focus on power
  – Microarchitecture improvements: deeper idle states, lower active power
  – Finer grain control: more voltage and frequency domains, improved power sharing
Resources

- ISA documentation for Haswell New Instructions
  - Intel® Architecture Instruction Set Extensions Programming Reference (PDF).
  - Intel®64 and IA-32 Architectures Software Developer Manuals.
- Software Developer Emulator (SDE)
  - Emulate new instructions before hardware is available
  - Intel® Software Development Emulator (Intel® SDE) (PDF)
- Intel® Architecture Code Analyzer
  - Code analysis for new instructions before hardware is available
  - Intel® Architecture Code Analyzer
- Intel® Compiler
  - Version 12.1 supports most Haswell New Instructions
  - Version 13.0 supports Intel® TSX
  - Intel® C++ Compiler
- Intel® VTune™ analyzer
  - New release will support Haswell PerfMON shortly after shipment
Q&A
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